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Cleopatra: a 12-channel recycling integrator ASIC for the readout of hydrogenated amorphous silicon detectors in radiotherapy dosimetry

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2025 JINST 20 C01034

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Abstract: The Cleopatra ASIC is a 12-channel prototype ASIC for the readout of hydrogenated amorphous silicon sensors used for real-time dosimetry in radiation diagnostic and radiation therapy. The architecture is based on a current to frequency conversion based on the recycling integrator principle in order to cover a dynamic range of four orders of magnitude with high linearity. Three different input amplifier configurations have been implemented in order to check the trade-off between detector capacitance and maximum output frequency. Cleopatra has been designed in CMOS 28 nm technology and succesfully tested in laboratory.

Keywords: Analogue electronic circuits; Digital electronic circuits; Front-end electronics for detector readout; Dosimetry concepts and apparatus

2025 JINST 20 C01034

Contents

2025 JINST 20 C01034

1 Introduction

Hydrogenated amorphous silicon (a-Si:H) is a promising material for high flux particle detection owing to its intrinsic radiation hardness and the possibility to deposit thin layers over a rigid or flexible substrate. In this framework, the INFN HASPIDE collaboration aims to the development of a-Si:H detectors for a number of applications ranging from X-ray dosimetry, solar high energy particle detection and neutron detection (coupled with a boron layer). One of the most promising applications is the dosimetry for Microbeam Radiation Therapy (MRT), where high dose-rate X-rays and spatially fractionated beams are combined in order to improve radiobiological effectiveness and treatment efficacy. Details on a-Si:H dectors developed by the HASPIDE collaboration for MRT are described in [1–3].

MRT dosimetry requires both a large dynamic range (between 100 pA and 2 µA) and a readout time below 400 µs, possibly down to 60 ns. In order to fulfill such requirements, a 12-channel ASIC prototype (named Cleopatra) has been developed in a commercial CMOS 28 nm technology. The ASIC is based on the recycling integration principle [4–7] in order to provide large dynamic range and direct digital output.

2 Readout architecture

The channel architecture, depicted in figure 1, features a high gain, high bandwidth input operational amplifier with a capacitor C_{INT} in feedback. The input current is integrated over C_{INT}, thus obtaining a voltage ramp at the amplifier output V_A. When the ramp crosses a threshold, a fixed amount of charge Q_{INJ} is subtracted from the amplifier input, thus changing V_A in the opposite direction by $\Delta V = Q_{INJ}/C_{INT}$. The measurement of the charge in a given time window can therefore be obtained by the product of the number of pulses generated during the time window multiplied by the amount of charge subtracted at each pulse.

As shown in figure 1, the subtracted charge is generated by sending the voltage pulse V_{QP}-V_{QN} to the capacitor C_{INJ}. Two fast current pulses of opposite polarity are thus generated. Depending on

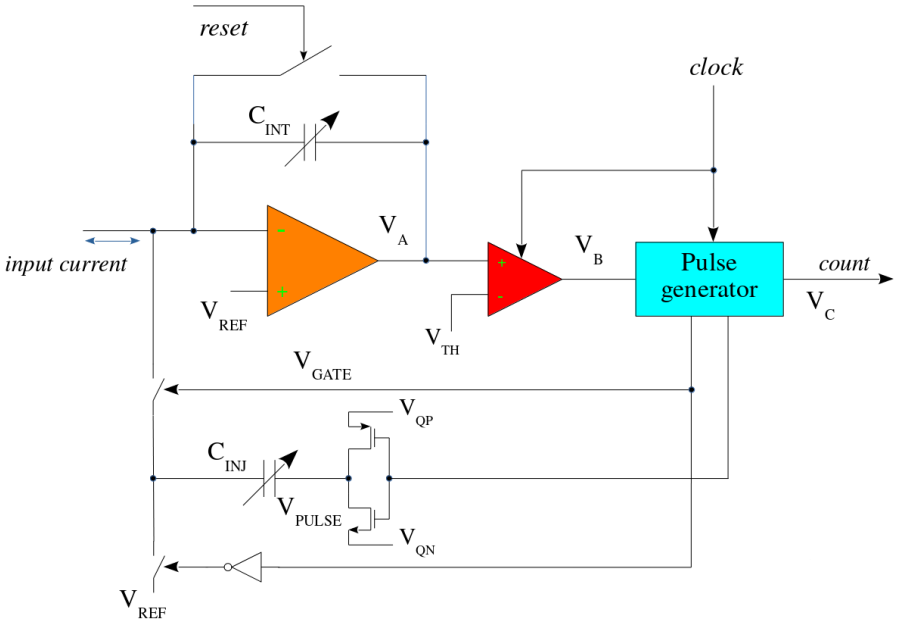

Figure 1. Readout channel schematic.

the input current polarity, one pulse is sent to the input while the other is discharged to V_{REF}. The overall behaviour is of a current to frequency converter with transfer function given by equation (2.1).

$$f_{OUT} = \frac{I_{in}}{Q_{INJ}} = \frac{I_{in}}{C_{INJ}(V_{QP} - V_{QN})} \tag{2.1}$$

The quantization error is thus given by the value of Q_{INJ}. One important property of this readout scheme is that the output frequency does not depend, at first order, from the offset of the operational amplifier and from the comparator threshold. On the other hand, it depends on the absolute value of an integrated capacitor, which can have variations of a few percent owing to process variation. A per-channel calibration of the injection charge is thus mandatory. The main limitation on the charge resolution is given by the parasitic capacitances, which limits the minimum C_{INJ} that can be used.

The pulse generator is a clocked finite state machine (FSM) which can produce a pulse every 4 clock cycles. The maximum current that the circuit can accept before saturation is therefore given by (2.2).

$$I_{MAX} = \frac{f_{CLK}}{4} C_{INJ}(V_{QP} - V_{QN}) \tag{2.2}$$

The maximum input current can be increased by increasing Q_{INJ} (thus worsening the resolution) or by increasing the clock frequency. It should be noted that the charge resolution is limited by the parasitic capacitance while the maximum current is limited by the clock frequency. Both factors can be significantly improved using an advanced technology node.

2.1 Input amplifier

The main limitation for the clock frequency is the input amplifier bandwidth. Three different operational amplifier configurations have been implemented: a two-stage cascoded amplifier with feed-forward compensation (FF), a current mirror configuration (CM) and a current mirror with gain boost (CMB) [8].

2025 JINST 20 C01034

Table 1. Operational amplifiers parameters.

Scheme	DC gain *[dB]*	GBW *[MHz]*	Power μW
FF	92	900	100
CM	42	240	30
CMB	74	260	90

The main parameters of the 3 amplifiers are summarized in table 1, where the usual trade-off between power consumption and performances can be observed. The choice of the amplifier architecture will be made on the base of the detector capacitance and the power budget.

The values of C_{INT} and C_{INJ} can be digitally programmed between 20 and 140 fF in 20 fF steps.

2.2 Digital interface

Each current to frequency converter is coupled to a 24-bit up/down counter, which in turn is connected to a 24 bit register, as shown in figure 2. An externally provided load signal, common to all registers, stores the value of the counters, thus providing a snapshot of the measured charge by all channels at a given time.

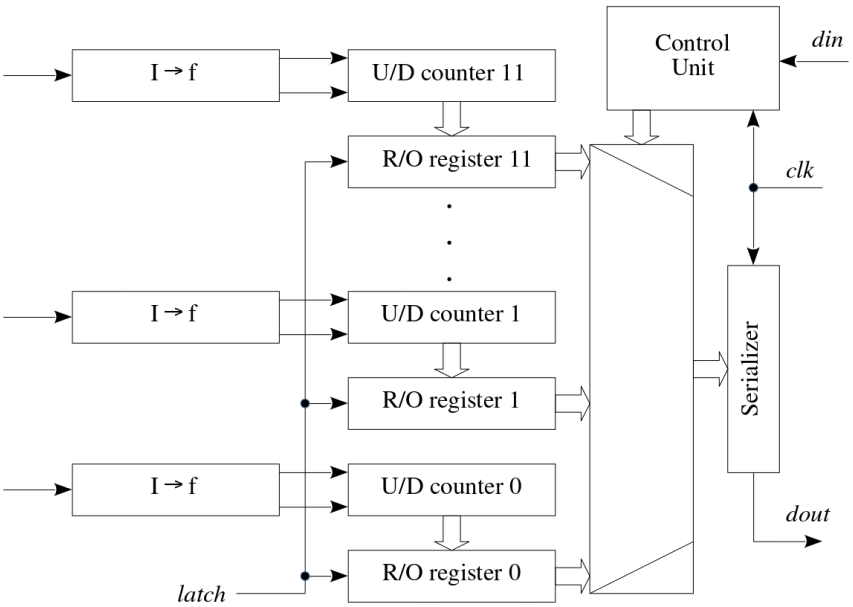

Figure 2. Digital interface.

The Cleopatra ASIC is controlled by a simple serial interface. A custom protocol based on two serial links (for input and output) working at half the clock frequency has been implemented. The input data format is based on 16-bit words, each divided in a 4-bit operational code and a 12-bit field. The protocol requires a continous stream of commands, started by a chip select word and ended by a chip deselect word. The possible command words are register select, register write, register read and no operation.

In the current prototype 7 configuration registers are implemented. They allows to set the channel polarities, the C_{INT} and C_{INJ} values and the tuning of the analog bias currents. Register 6 defines the register (either control or data) to be read-out by a read register command. The output data format is based on 32-bit words with a 4-bit header, a 24-bit data field and a 4-bit trailer.

3 Cleopatra prototype

The first prototype of the Cleopatra ASIC has been designed in a commercial 28 nm CMOS technology. The prototype includes 12 current-to-frequency converters (four channels for each input amplifier configuration), a bank of 12×24 bit counters and registers, and the digital control logic implementing the readout and configuration protocol.

The die size is 1.1×1.3 mm^2. The prototype is designed to work at clock frequencies up to 640 MHz. The digital interface is based on custom SLVS drivers and receivers [9]. The ASIC requires two supply voltages, at 0.9 V for the core and 1.5 V for the pads.

4 Test results

The ASIC has been tested standalone by providing a precise voltage with a Source Measurement Unit (SMU) and measuring the current with the same instrument. A 10 MΩ resistor mounted on the test PCB in series to the input provides a high impedance source. The digital interface is controlled by an FPGA-based evaluation board connected to a computer via ethernet interface. Owing to limitation of the FPGA, the test has been performed with a clock frequency of 500 MHz.

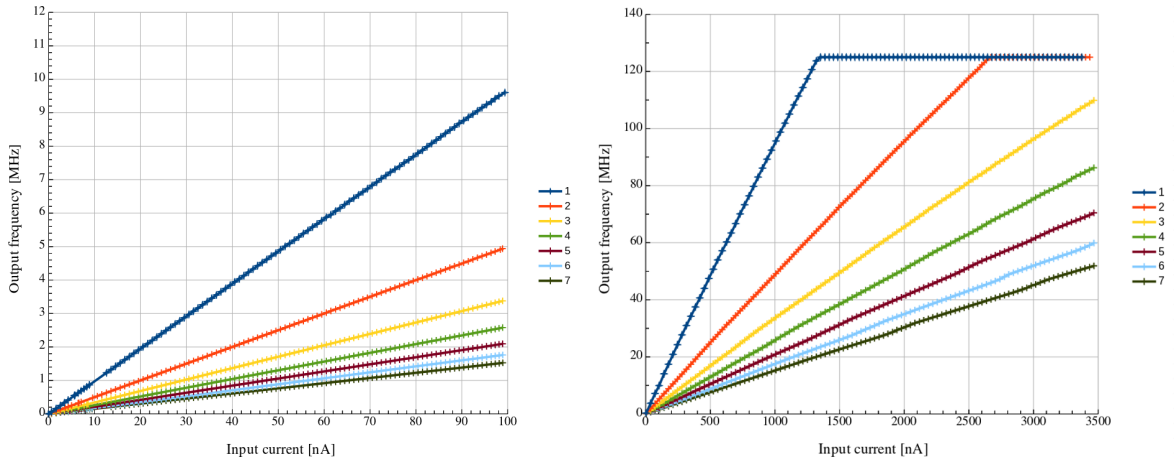

Figure 3. Channel linearity.

Figure 3 (left) shows converter transfer function for the 7 injection capacitance configurations, corresponding to capacitors between 20 and 140 fF. The ΔV_Q was set to 600 mV. The non-linearity is below ±0.5% for currents above a few nA. The same tests have been performed with a input series resistance of 1 MΩ, testing the range up to 3.5 µA, as shown in figure 3 (right). A non-linearity below ±2% has been measured in this range. As expected, the circuit saturates at 125 MHz, i.e. one quarter of the clock frequency.

Figure 4 (left) shows the charge injection value measured as linear fit of the transfer function for 11 channels, compared with the nominal value. It can be observed that it is fairly homogeneous among

2025 JINST 20 C01034

channels. On the other hand, it is significantly different from the nominal one. Possible reasons of this discrepancies can be process spread of the capacitor value, effect of parasitic capacitance and voltage drop on the V_Q lines. Further investigations are ongoing to identify the reason of this discrepancy.

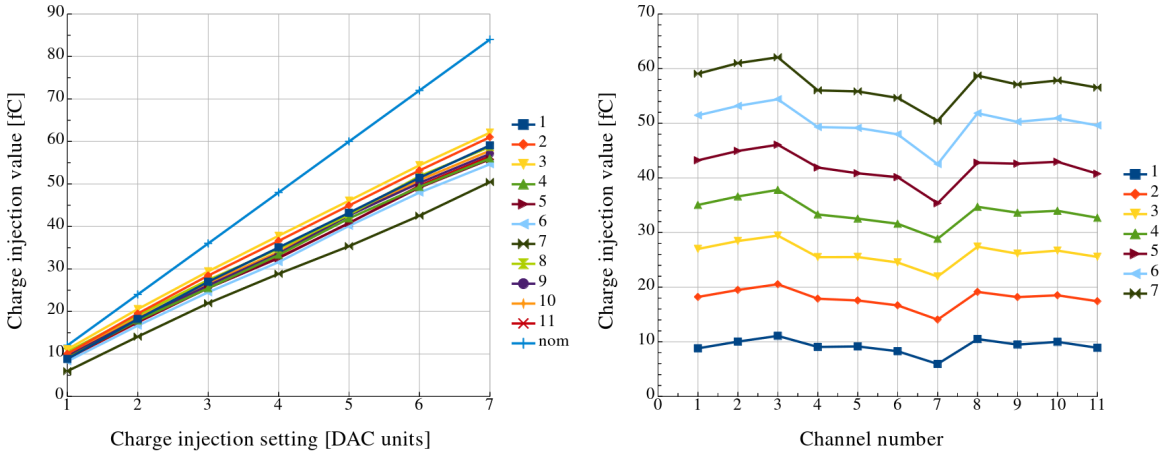

Figure 4. Charge quantum measurement.

Further tests are planned to explore the current range below 10 nA and to verify the Cleopatra performances coupled with a aSi:H detector. The design of the final, 32-channel Cleopatra has started and is expected to be submitted in the second quarter of 2025.

5 Conclusions

A 12-channels large dynamic range ASIC based on the recycling integrator principle has been designed in a commercial CMOS 28 nm technology and tested. First results confirm very good linearity in the range down to a few nA, while more tests are required to evaluate the circuit performances below this value. A significant discrepancy between the nominal and measured charge quantum value is under investigation. Further tests are ongoing in order to complete the characterization. The final, 32-channel version of the ASIC will be submitted in the second quarter of 2025.

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2025 JINST 20 C01034